In the Claims:

1.-10. (Canceled)

11. (Currently Amended) A method of fabricating a transistor, the method comprising:

providing a workpiece, the workpiece having a top surface;

implanting germanium into the top surface of the workpiece so that the highest concentration of germanium is at the top surface of the workpiece with the concentration gradually decreasing as the distance from the top surface increases, said implanting further forming a first germanium-containing region extending from ~~within~~ the top surface of the workpiece, ~~workpiece~~ and forming a second germanium-containing region beneath the first germanium-containing region, the first germanium-containing region extending a first depth beneath the workpiece top surface, the second germanium-containing region having a second depth extending below the first depth, the first and second depth comprising about 100 Å or less below the top surface of the workpiece;

depositing a gate dielectric material over the first germanium-containing region;

depositing a gate material over the gate dielectric material;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric over the first germanium-containing region; and

forming a source region and a drain region in at least the first germanium-containing region.

12. (Original) The method according to Claim 11, wherein forming the first germanium-containing region comprises forming an amorphous germanium-containing region, and wherein

forming the second germanium-containing region comprises forming a first crystalline germanium-containing region.

13. (Original) The method according to Claim 12, further comprising annealing the workpiece, before depositing the gate dielectric material, converting the amorphous germanium-containing region to a second crystalline germanium-containing region, the first crystalline germanium-containing region and the second crystalline germanium-containing region comprising a single crystalline germanium-containing region, the single crystalline germanium-containing region comprising a third depth beneath the workpiece top surface.

14. (Original) The method according to Claim 13, wherein the third depth is about 120 Å or less.

15. (Original) The method according to Claim 13, wherein the first depth is about 45 Å or less, and the second depth is about 55 Å or less.

16. (Original) The method according to Claim 13, whercin annealing the workpiece comprises heating the workpiece to a temperature of about 750 °C or less for about 60 minutes or less.

17. (Original) The method according to Claim 12, further comprising anncaling the workpiece, after depositing the gate dielectric material, converting the amorphous germanium-containing region to a second crystalline germanium-containing region, the first crystalline

germanium-containing region and the second crystalline germanium-containing region comprising a single crystalline germanium-containing region, the single crystalline germanium-containing region comprising a third depth beneath the workpiece top surface.

18. (Original) The method according to Claim 17, wherein the third depth is about 120 Å or less.

19. (Original) The method according to Claim 17, wherein the first depth is about 45 Å or less, and the second depth is about 55 Å or less.

20. (Original) The method according to Claim 17, wherein annealing the workpiece comprises heating the workpiece to a temperature of about 750 °C or less for about 60 minutes or less.

21. (Original) The method according to Claim 12, wherein implanting germanium into the top surface of the workpiece comprises forming a damage region between the first germanium-containing region and the second germanium-containing region, further comprising annealing the workpiece, converting the amorphous germanium-containing region to a second crystalline germanium-containing region, the first crystalline germanium-containing region and the second crystalline germanium-containing region comprising a single crystalline germanium-containing region, and wherein annealing the workpiece causes the removal of the damaged region between the first germanium-containing region and the second germanium-containing region.

22. (Original) The method according to Claim 11, wherein implanting the germanium comprises implanting germanium at an energy dose of about 5 keV or less.

23. (Original) The method according to Claim 11, wherein implanting the germanium comprises implanting germanium at a dose of about 1×10^{15} to 1×10^{17} atoms/cm^2.

24. (Currently Amended) The method according to Claim 11, wherein the step of implanting the germanium into said ~~comprises forming the~~ first germanium-containing region comprising implanting a portion of said first germanium containing region with at least 80% germanium ~~at a top portion thereof~~.

25. (Currently Amended) The method according to Claim 24, wherein the step of implanting the germanium into said ~~comprises forming the~~ first germanium-containing region comprising implanting a portion of said first germanium containing region with substantially 100% germanium ~~at a top portion thereof~~.

26. (Original) The method according to Claim 11, wherein depositing the gate dielectric material comprises depositing a material having a dielectric constant of about 4.0 or greater.

27. (Original) The method according to Claim 26, wherein the depositing the gate dielectric material comprises depositing HfO_2, $HfSiO_X$, Al_2O_3, ZrO_2, $ZrSiO_X$, Ta_2O_5, La_2O_3, Si_xN_y, SiON, or combinations thereof.

28. (Original) The method according to Claim 11, wherein depositing the gate dielectric material comprises depositing SiO_2.

29. (Original) The method according to Claim 11, further comprising forming isolation regions in the workpiece, before implanting germanium into the top surface of the workpiece.

30. (Original) The method according to Claim 11, further comprising forming spacers over sidewalls of the gate and gate dielectric.

31. (Original) The method according to Claim 11, wherein providing the workpiece comprises providing a silicon-on-insulator (SOI) wafer.

32. (Original) The method according to Claim 11, wherein forming the source and drain regions comprises a temperature of about 938.3 °C or less.

33. (Original) A method of fabricating a transistor, the method comprising:

providing a workpiece, the workpiece having a top surface;

implanting germanium into the top surface of the workpiece, forming an amorphous germanium-containing region within the top surface of the workpiece, the amorphous germanium-containing region extending about 45 Å or less beneath the workpiece top surface, wherein implanting germanium into the top surface of the workpiece also forms a first crystalline germanium-containing region beneath the amorphous germanium-containing region, the first crystalline germanium-containing region extending about 55 Å or less beneath the amorphous germanium-containing region;

depositing a gate dielectric material over the amorphous germanium-containing region, the gate dielectric material having a dielectric constant of about 4.0 or greater;

annealing the workpiece at a temperature of about 750 °C or less for about 60 minutes or less, re-crystallizing the amorphous germanium-containing region and forming a single second crystalline germanium-containing region within the top surface of the workpiece, the single second crystalline germanium-containing region comprising the re-crystallized amorphous germanium-containing region and the first crystalline germanium-containing region, the second crystalline germanium-containing region extending about 120 Å or less beneath the workpiece top surface;

depositing a gate material over the gate dielectric material;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric over the second crystalline germanium-containing region; and

forming a source region and a drain region in at least the second crystalline germanium-containing region.

34. (Original) The method according to Claim 33, wherein implanting the germanium into the top surface of the workpiece comprises forming a damage region between first germanium-containing region and the second germanium-containing region, further comprising annealing the workpiece, converting the amorphous germanium-containing region to a second crystalline germanium-containing region, the first crystalline germanium-containing region and the second crystalline germanium-containing region comprising a single crystalline germanium-containing region, and wherein annealing the workpiece causes the removal of the damaged region between the first germanium-containing region and the second germanium-containing region.

35. (Original) The method according to Claim 33, wherein implanting the germanium comprises implanting germanium at an energy dose of about 5 keV or less and at a dose of about 1×10^{15} to 1×10^{17} atoms/cm^2.

36. (Original) The method according to Claim 33, wherein implanting the germanium comprises forming the first germanium-containing region comprising at least 50% germanium at a top portion thereof.

37. (Original) The method according to Claim 33, wherein the depositing the gate dielectric material comprises depositing HfO_2, $HfSiO_X$, Al_2O_3, ZrO_2, $ZrSiO_X$, Ta_2O_5, La_2O_3, Si_xN_y, SiON, or combinations thereof.

38. (Original) The method according to Claim 33, wherein forming the source and drain regions comprises a temperature of about 938.3 °C or less.